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(56) Documents cited
GB 2213027 A GB 2111803 A GB 2064918 A
GB 2049365 A EP 0212424 A2 EP 0184816 A2
WO 80/01008 A1 US 5081440 A

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UK CL (Edition L) H4P PPC
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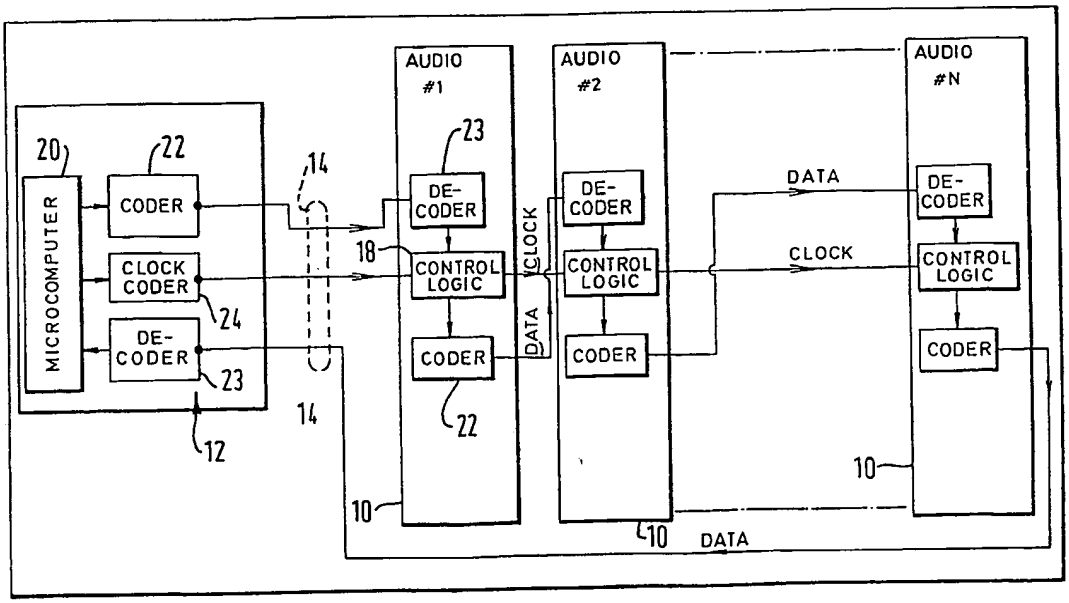
(54) Reducing crosstalk in networks

(57) A modular electrical circuit includes, for example, a number of audio modules (10) serially interconnected by way of ribbon cables (14) and respective connectors (16). The first and last audio modules (10) are each connected to a digital controller (12) to define a serial loop. To minimize the risk of cross talk between the digital signals and the audio modules, the serial loop is formed such that each said module is coupled to the preceding module (10) or to the digital control means (12) in such a manner that the output of one module is not directly connected to the output of a preceding or succeeding module. For example, in an arrangement utilizing a single bus, physical discontinuities are formed in selected lines of the bus at selected positions to provide open circuits, Fig. 3, (not shown).

FIG.1



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIG. 1

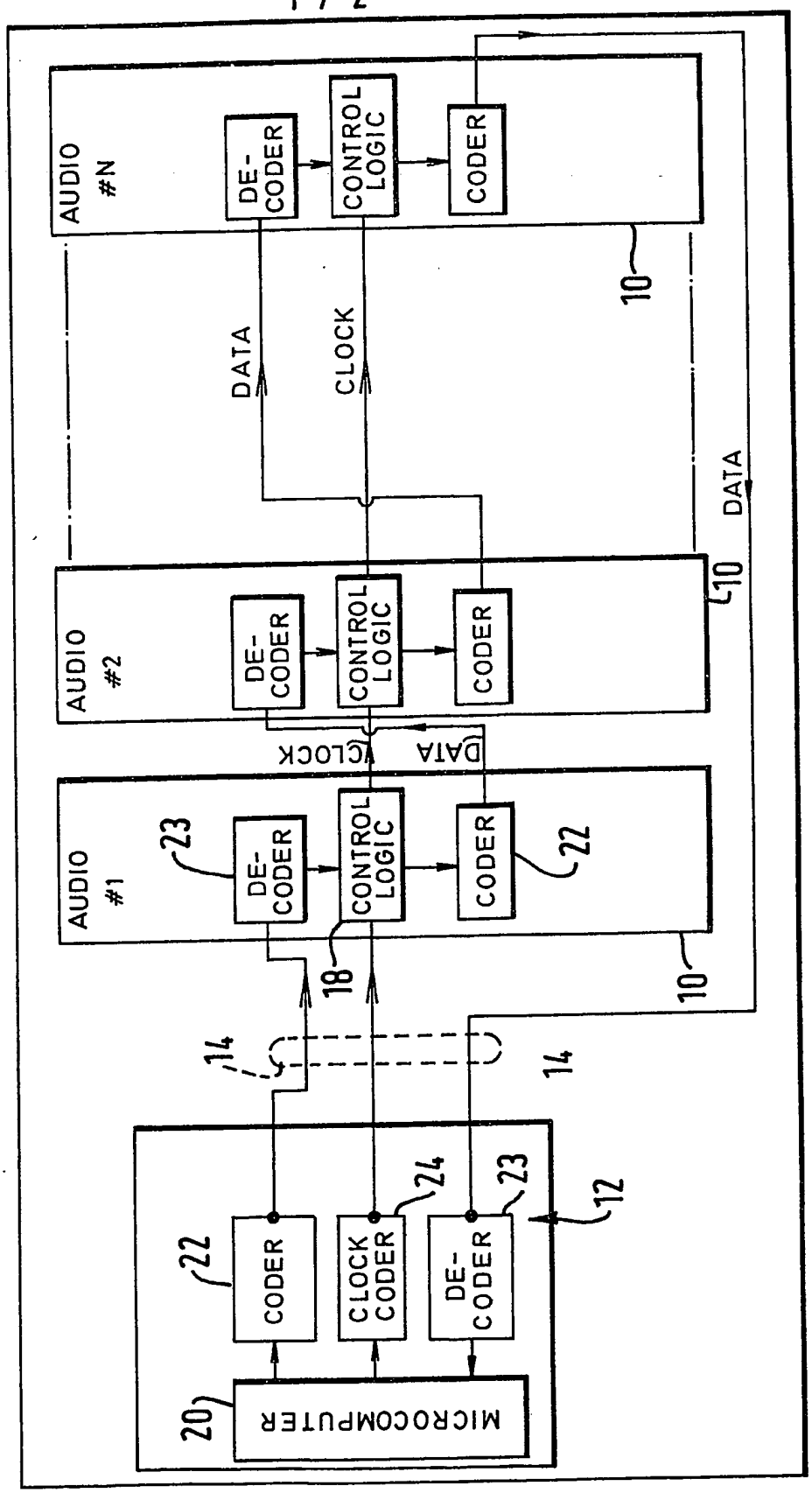

AUDIO #N
DE-CODER
CONTROL LOGIC
CODER
10
DATA
CLOCK
AUDIO #2
AUDIO #1
23
22
18
14
MICROCOMPUTER
20
CLOCK CODER
24
12

FIG. 2

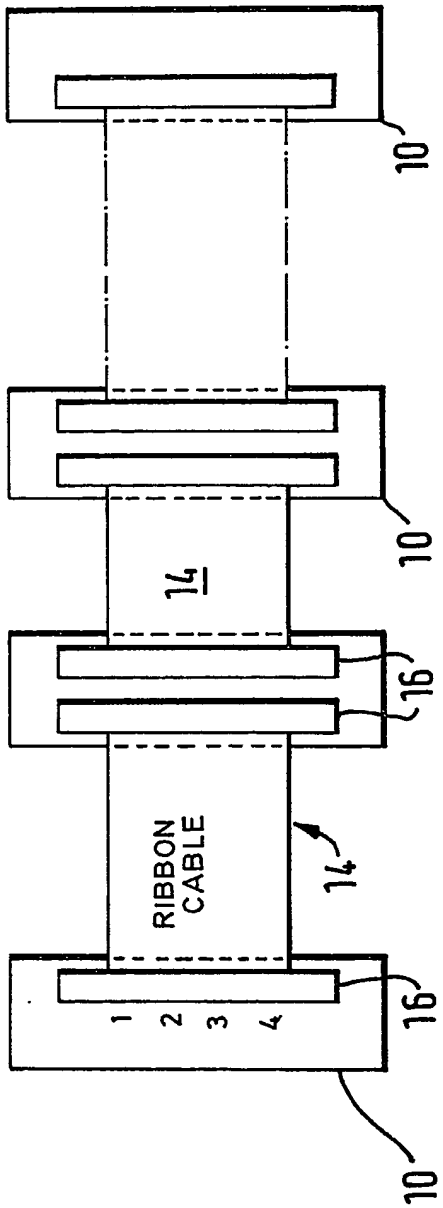
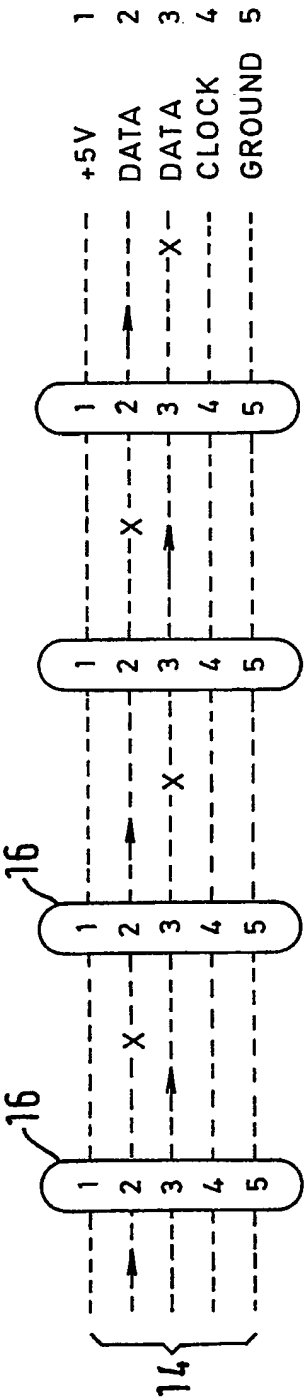

10
10
14
16
RIBBON CABLE
14
16
1 2 3 4
10

FIG. 3


1 +5V
2 DATA
3 DATA
4 CLOCK
5 GROUND
16
16
14

IMPROVEMENTS IN OR RELATING TO NETWORKS

The present invention relates to networks, and to modular electrical circuits incorporating a ring network. For example, the invention particulary relates to serial networks for analogue systems incorporating digital control means.

Digital techniques are becoming increasingly sophisticated, and it is required to control analogue systems by digital circuits. However, analogue systems, such as audio mixing consoles, for example, are particularly susceptible to all forms of noise and standard digital control techniques generally generate tones and whistles on the audio output.

In our British patent application No. 9205291.9 we disclosed methods for disguising noise emanating from the digital signals. However, it is also useful to arrange the topology of the circuits to avoid or minimize coupling between digital lines and audio circuits.

According to a first aspect of the present invention there is provided a network comprising at least one bus, and at least two connectors coupled to said bus to receive signals from the bus and to impart signals thereto, wherein each of said connectors is substantially identical, and wherein the arrangement is such that the output of each said connector is not directly connected to the output of an adjacent connector.

In a preferred embodiment, direct coupling between outputs of adjacent connectors is prevented by open circuits in selected lines of said bus. For example, the open circuits in the selected lines of said bus may be formed by physical discontinuities in the selected lines.

The physical discontinuities in the lines of the bus may be formed, for example, by jig punching.

Preferably, the connectors and the or each bus define a serial loop or ring network interconnecting two or more modules arranged to receive and/or impart data to said bus or buses by way of respective connectors. It is preferred that the bus is unitary and that each said module has a single said connector connected to said bus. Generally, the bus will be defined by a single ribbon cable.

In an embodiment, selected pins of each connector are designated as data carrying pins and are connected to data lines of said bus, the same pins being designated as data carrying in each said connector.

Preferably, control logic means are provided to selectively set the data receiving and/or data imparting condition of data carrying pins of the connectors.

In one embodiment, respective control logic means is incorporated in each said module and is arranged, on detecting the arrival of data at one data carrying pin of its associated connector, to set a different data carrying pin thereof as a data output pin.

The invention also extends to a modular electrical circuit comprising one or more serially coupled modules defining a serial loop, wherein each said module is coupled to a preceding module by a bus, and wherein the bus is arranged so that the output of one module is not directly connected to the output of a preceeding or succeeding module.

For example, the bus may be arranged to define a ring network and may be coupled to each said module by way of

substantially identical connectors, and wherein an open circuit is connected to an output pin of each said connector, the open circuit being connected to different output pins of adjacent connectors.

In a preferred embodiment, the bus is a unitary bus and is defined by a single ribbon cable.

In a preferred embodiment, one of the pins of the connector coupled to each said module is dedicated as an input port, and another of the pins of said connector is dedicated as an output port, and wherein the connectors of adjacent modules have different ones of their connector pins dedicated as input and output ports.

In a preferred embodiment, said modules comprise a plurality of serially connected audio components coupled to digital control means to define the serial loop.

In a preferred embodiment, said digital control means comprises a controller which comprises or is coupled to processing means, for example, a microprocessor.

In a preferred embodiment, the controller is serially coupled to the one or a first one of said audio components. Preferably, the audio system is a modular system formed of the plurality of serially coupled audio components, the first one of which is coupled to said controller, and a last one of which is also connected to said controller to define the serial loop.

Preferably, each said audio component comprises a decoder for receiving coded digital signals from the controller or a preceding audio component, and preferably each said audio component comprises a coder for coding digital signals and transmitting them to a succeeding audio

component or said controller.

The decoder of each said audio component is coupled by said bus to a preceding audio component or to the controller, and the coder of each said audio component is coupled to a succeeding audio component or to the controller.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows schematically an audio analogue system of the invention incorporating digital control means,

Figure 2 shows a first method of connecting audio modules of the analogue system of Figure 1 to each other and to a controller to form a network in accordance with the present invention, and

Figure 3 shows schematically a further method for interconnecting modules of the analogue system to form a network in accordance with this invention.

Because of the power and accuracy of digital techniques, it is required to use digital control for analogue systems. However, where the analogue system to be controlled is, or incorporates, audio modules or components, the digital signals inevitably produce tones and whistles on the audio output which are quite unacceptable. In this respect, the signals produced by digital circuits are generally pulsed waveforms with fast rise and fall times. Such signals are rich in harmonics up to frequencies as high as several hundred megahertz. The sharper the transitions of the pulse waveform, the higher in frequency the harmonics extend.

If the fundamental frequency of a digital signal is within the audio band it may be directly audible at the

audible output. Furthermore, there may be intermodulation effects between any one of the harmonics of the digital signal and any other radio frequency component present. This intermodulation can produce significant interference in the audio band.

The unwanted signals from the digital controller can be coupled into the analogue system by crosstalk, that is, by capacitive or inductive coupling, by electromagnetic radiation coupling, or by the existence of common impedance paths. Clearly, such coupling can be minimised by careful positioning of the digital lines relative to the audio circuits, by screening, and by the provision of isolation circuits and the like.

Even when the circuits have been subjected to the most rigorous constructional techniques to avoid coupling there are still problems. In this respect, the digital signals generate single coherent tones, and the human ear readily detects such coherent tones, even amongst a background of white noise which is at a much higher level than the tones themselves. The applicants have determined that a tone must be 20dB lower than the surrounding noise before it becomes imperceptible. The applicants have proposed to disguise the control waveforms rather than to try to eliminate them and their proposals are described in our copending British applications which also claim priority from our British patent application No. 9205291.9. In this respect, the digital control signals are arranged to appear as white noise which is rendered indistinguishable from the white noise generated by the analogue circuitry. This is done by randomising or scrambling the digital signals such that these are not cyclic or repetitive.

Figure 1 shows schematically an audio mixing console controlled by digital control means incorporating the

disguise techniques described in the applicants above referenced British patent application. This audio mixing console also incorporates a network topology of the present invention.

The illustrated audio mixing console incorporates N audio components or modules 10, each generally providing one channel of the console. The components and functions of each audio module 10 may be chosen as required. However, each said audio module 10 will generally comprise at least one shift register to receive digital data and fader circuits controlled by the or each shift register. The faders will be arranged to adjust controllable audio amplifiers by way of appropriate digital to analogue conversion circuits.

In the embodiment illustrated, each audio module 10 is connected in series to the other audio modules 10, with the first module being 10 serially connected to a digital control circuit or controller 12, and the last module 10 being similarly connected to the digital controller 12. The arrangement is such as to provide a serial loop, and the logic of the controller and/or of the modules is arranged such that data passes around the serial loop in one direction only, that is, so that the serial loop is unidirectional.

The structure and functions of the digital controller 12 may be determined as convenient. The controller 12 is arranged to provide digital signals to the audio modules 10, the digital signals comprising both clock signals and data. In the illustrated embodiment, the digital controller 12 includes processing means 20 to generate the data. Alternatively, the digital controller may be connected to receive the data from external means. However, because the controller 12 is a digital circuit, it

is physically isolated in the console from the audio modules 10.

In the embodiment illustrated, the controller 12 comprises a data coding circuit 22 which is arranged to randomise data and transmit it to the audio modules 10. In this respect, each audio module 10 is provided with a respective data decoder 23. The controller 12 is also provided with a clock coder 24 which is arranged to randomise or scramble clock signals which are fed to the audio modules 10. The controller 12 also comprises a data decoder 23 which is substantially identical in construction to respective decoders 23 of the audio modules 10.

As is shown in Figure 2, the serial loop is physically provided by way of a ribbon cable 14 which interconnects a connector 16 of the controller 12 and substantially identical connectors 16 of the audio modules 10. To form the serial loop, each audio module 10 is provided with two identical connectors 16. In the embodiment illustrated in Figure 2, a first designated pin of each connector 16 is arranged to carry the ground, the third and fourth pins of each connector 16 are arranged to carry data, and the fourth pin of each connector 16 is selected to carry the coded clock signal from the clock coder 24 which is applied to the respective pin of each connector 16 by way of the ribbon cable 14 and hence to a respective control logic circuit 22 of each said audio module 10.

It will be immediately apparent from Figure 1 that as well as having a data decoder 23 for the data, each audio module 10 also has a data coder 22. The data coder 22 of each module 10 is substantially identical to the data coder 22 of the controller 12. Thus, at each audio module 10 the data received is decoded for use by that module, and is also encoded for transmission to the next module. This

means that the data is always transmitted in its coded, randomised form, and also that the data is only decoded directly at its point of use. This reduces considerably the opportunity for crosstalk or any interference from the uncoded data.

It will also be appreciated that the coded clock signals from the clock coder 24 of the controller 12 are applied to control logic 18 of each audio module 10 for control of that module. Furthermore, the control logic 18 of one audio module 10 passes on the coded clock signal to the next audio module 10. As the clock signals are transmitted through the console in randomised form, the opportunity for interference or intermodulation is considerably reduced. The nature of the data and clock encoding and decoding is outside the scope of this application and is not further discussed herein. It is described in detail in the aforementioned British patent applications which also claim priority from our patent application No. 9205291.9.

In the embodiment described and illustrated above in Figures 1 and 2, the serial loop is formed by providing two connectors 16 in each audio module 10 for connection respectively to the preceding and succeeding modules in the chain. An individual ribbon cable 14 is required to connect each pair of connectors. In this respect, the arrangement is such that the data output pin of the connector 16 of one module, either audio module 10 or controller 12, is not directly coupled to the data output pin of the adjacent connector 16. Thus, the third pin of each connector 16 is designated as a receive data, or input pin, of each connector 16 whilst the fourth pin thereof is the data output pin, or send data pin. This arrangement prevents the formation of common impedance paths and minimizes crosstalk.

However, for manufacturing ease, it is preferred to have a single ribbon cable which runs along all of the modules and which is connected to each module 10 by a single connector. However, if, as is also preferred, each module has the same arrangement of output pins, such an arrangement would mean that all of the outputs of all of the modules would be connected together as would all of their inputs.

Figure 3 illustrates a further embodiment of the invention and shows how a ring topology can be provided in these circumstances. In fact, neither topology illustrated in the Figures of this application is limited to the control of audio modules by a controller. The ring topology of Figure 3, for example, can be utilised in any network where a ring is required and the nodes on the ring are identical.

Figure 3 shows schematically a bus provided by the use of a ribbon cable 14. Five lines of the cable 14 are indicated as lines 1 to 5 and, as illustrated line 1 will carry the power, line 4 will carry the clock, and line 5 will carry the ground. The lines are all connected to respective ones of the pin of respective connectors 16. Each module, as 10 of Figure 1, has a respective connector 16 which, and as indicated in Figure 3, has 5 pins each of which is connected to a respective line of the ribbon cable 14. However, and as is indicated by a cross, open circuits are provided on the data carrying lines 2 and 3 at alternate positions. These open circuits may be provided by physical discontinuities in the lines, for example, formed by way of jig punching. Arrow heads in Figure 3 show the path for the transmission of serial data.

Consideration of Figure 3 will show that data flows into the first connector 16 at the upstream end on pin 2

but outputs that connector on pin 3. The data arriving at the succeeding connector 16 on pin 3 thereof flows out of the connector on pin 2 and so on. With this arrangement it will be appreciated that the output of one module, for example on pin 3 of the associated connector, is not directly connected to the output of the next module, for example to the output on pin 2 of the succeeding connector, because of the interposition of an open circuit.

The flow of data can be determined automatically. Thus, each of the pins 2 and 3 of each connector may automatically set to 'IN' on reset. Control logic can then be arranged, upon detecting arriving data on one pin, say on pin 2, to automatically set the other pin, say 3, to 'OUT'.

Preferably, the respective control logic circuit 18 provided in each said audio module 10 is arranged to set the connector pins 2 and 3 of the respective connector 16. However, if required, dedicated control logic may be associated with each said connector 16.

Other variations and modifications to the particular embodiments described above may be made within the scope of this application.

CLAIMS

1. A network comprising at least one bus, and at least two connectors coupled to said bus to receive signals from the bus and to impart signals thereto, wherein each of said connectors is substantially identical, and wherein the arrangement is such that the output of each said connector is not directly connected to the output of an adjacent connector.

2. A network as claimed in Claim 1, wherein direct coupling between outputs of adjacent connectors is prevented by open circuits in selected lines of said bus.

3. A network as claimed in Claim 2, wherein the open circuits in the selected lines of said bus are formed by physical discontinuities in the selected lines.

4. A network as claimed in any preceding claim, wherein the connectors and the or each bus define a serial loop or ring network interconnecting two or more modules arranged to receive and/or impart data to said bus or buses by way of respective connectors.

5. A ring network as claimed in Claim 4, wherein only a single bus is provided, and wherein each said module has a single said connector connected to said bus.

6. A ring network as claimed in Claim 5, wherein selected pins of each connector are designated as data carrying pins and are connected to data lines of said bus, the same pins being designated as data carrying in each said connector.

7. A ring network as claimed in Claim 6, further comprising control logic means to selectively set the data

receiving and/or data imparting condition of data carrying pins of said connectors.

8. A ring network as claimed in Claim 7, wherein respective control logic means is incorporated in each said module and is arranged, on detecting the arrival of data at one data carrying pin of its associated connector, to set a different data carrying pin thereof as a data output pin.

9. A modular electrical circuit comprising one or more serially coupled modules defining a serial loop, wherein each said module is coupled to a preceding module by a bus, and wherein the bus is arranged so that the output of the module is not directly connected to the output of a preceding or succeeding module.

10. A modular electrical circuit as claimed in Claim 9, wherein the bus is arranged to define a ring network and is coupled to each said module by way of substantially identical connectors, and wherein an open circuit is connected to an output pin of each said connector, the open circuit being connected to different output pins of adjacent connectors.

11. A modular electrical circuit as claimed in Claim 10, wherein the bus is defined by a single ribbon cable.

12. A modular electrical circuit as claimed in Claim 10 or 11, wherein one of the pins of the connector coupled to each said module is dedicated as an input port, and another of the pins of said connector is dedicated as an output port, and wherein the connectors of adjacent modules have different ones of their connector pins dedicated as input and output ports.

13. A modular electrical circuit as claimed in any of

Claims 9 to 12, wherein said modules comprise a plurality of serially connected audio components coupled to digital control means to define the serial loop.

14. A modular electrical circuit as claimed in Claim 13, wherein said digital control means comprises a controller which comprises or is coupled to processing means, and wherein the controller is serially coupled to the one or a first one of said audio components, and a last one of said audio components is also connected to said controller to define the serial loop.

15. A modular electrical circuit as claimed in Claim 14, wherein each said audio component comprises a decoder for receiving coded digital signals from the controller or a preceding audio component, and each said audio component comprises a coder for coding digital signals and transmitting them to a succeeding audio component or said controller, and wherein the decoder of each said audio component is coupled by said bus to a preceding audio component or to the controller, and the coder of each said audio component is coupled by said bus to a succeeding audio component or to the controller.

16. A network substantially as hereinbefore described with reference to the accompanying drawings.

17. A modular electrical circuit substantially as hereinbefore described with reference to the accompanying drawings.

atents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
GB 9304978.1

Relevant Technical fields

(i) UK Cl (Edition L) H4P (PPC)

(ii) Int Cl (Edition 5) H04L 12/10, 12/40, 12/42

Search Examiner
K WILLIAMS

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
11 MAY 1993

Documents considered relevant following a search in respect of claims 1-15

Category (see over)	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2213027 A	(TEXAS INSTRUMENTS) See Figure 2	1, 9
X	GB 2111803 A	(ICL) See Claim 1	1, 9
X	GB 2064918 A	(BRITISH AEROSPACE) See abstract	1, 9
X	GB 2049365 A	(STC) See abstract	1, 9
X	EP 0212424 A2	(HITACHI) See column 3, lines 12-15; and US 4697047	1, 9
X	EP 0184816 A2	(HONEYWELL INC) See abstract	1, 9
X	WO 80/01008 A1	(CHRISTIAN ROUSING) See abstract; and GB 2055276 A	1, 9
X	US 5081440	(SIEMENS) See column 2, lines 8ff; and EP 0365696 A1	1, 9

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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